

WHAT IS CLAIMED IS:

1 1. A multiplier circuit comprising:

2 a partial products generating circuit capable of
3 receiving a multiplicand value and a multiplier value and
4 generating therefrom a plurality of partial products;

5 a first summation array circuit comprising a first
6 plurality of adders capable of summing a first subset of said
7 plurality of partial products to thereby produce a first summation
8 value; and

9 a second summation array circuit comprising a second
10 plurality of adders capable of summing a remaining subset of said
11 plurality of partial products to thereby produce a second summation
12 value, wherein said remaining subset of said plurality of partial
13 products comprises all of said plurality of partial products not
14 included in said first subset of said plurality of partial
15 products.

1 2. The multiplier circuit as set forth in Claim 1 wherein
2 said first subset comprises even ones of said plurality of partial
3 products.

1 3. The multiplier circuit as set forth in Claim 2 wherein
2 said remaining subset comprises odd ones of said plurality of
3 partial products.

1 4. The multiplier circuit as set forth in Claim 3 wherein
2 each of said first and second pluralities of adders comprises a
3 carry-save adder.

1 5. The multiplier circuit as set forth in Claim 4 further
2 comprising a final stage carry-save adder capable of summing said
3 first summation value and said second summation value.

1 6. The multiplier circuit as set forth in Claim 5 wherein
2 said first summation value comprises a first N-bit sum value and a
3 first N-bit carry value and said second summation value comprises
4 a second N-bit sum value and a second N-bit carry value and wherein
5 said final stage carry-save adder compresses said first and second
6 summation values to produce a final summation value comprising a
7 final N-bit sum value and a final N-bit carry value.

1 7. The multiplier circuit as set forth in Claim 6 further
2 comprising a carry-propagate adder capable of adding said final N-
3 bit sum value and said final N-bit carry value to produce a 64-bit
4 resulting sum value and a 1-bit resulting carry value.

1 8. The multiplier circuit as set forth in Claim 7 wherein
2 said multiplier circuit is disposed in at least one of a floating
3 point unit and an integer unit in a data processor.

1 9. A data processor comprising a plurality of pipelined
2 execution units, said pipelined execution units comprising at least
3 one of a floating point unit and an integer having at least one
4 multiplier circuit therein, wherein said at least one multiplier
5 circuit comprises:

6 a partial products generating circuit capable of
7 receiving a multiplicand value and a multiplier value and
8 generating therefrom a plurality of partial products;

9 a first summation array circuit comprising a first
10 plurality of adders capable of summing a first subset of said
11 plurality of partial products to thereby produce a first summation
12 value; and

13 a second summation array circuit comprising a second
14 plurality of adders capable of summing a remaining subset of said
15 plurality of partial products to thereby produce a second summation
16 value, wherein said remaining subset of said plurality of partial
17 products comprises all of said plurality of partial products not
18 included in said first subset of said plurality of partial
19 products.

1 10. The data processor as set forth in Claim 9 wherein said
2 first subset comprises even ones of said plurality of partial
3 products.

1. 11. The data processor as set forth in Claim 10 wherein said
2 remaining subset comprises odd ones of said plurality of partial
3 products.

1. 12. The data processor as set forth in Claim 11 wherein each
2 of said first and second pluralities of adders comprises a carry-
3 save adder.

1. 13. The data processor as set forth in Claim 12 further
2 comprising a final stage carry-save adder capable of summing said
3 first summation value and said second summation value.

1. 14. The data processor as set forth in Claim 13 wherein said
2 first summation value comprises a first N-bit sum value and a first
3 N-bit carry value and said second summation value comprises a
4 second N-bit sum value and a second N-bit carry value and wherein
5 said final stage carry-save adder compresses said first and second
6 summation values to produce a final summation value comprising a
7 final N-bit sum value and a final N-bit carry value..

1 15. The data processor as set forth in Claim 14 further
2 comprising a carry-propagate adder capable of adding said final N-
3 bit sum value and said final N-bit carry value to produce a 64-bit
4 resulting sum value and a 1-bit resulting carry value.

1 16. The data processor as set forth in Claim 15 wherein said
2 at least one multiplier circuit comprises a first multiplier
3 disposed in said floating point unit and a second multiplier
4 disposed in said integer unit.

1 17. For use in a data processor, a method of multiplying a
2 multiplicand value and a multiplier value comprising the steps of:

3 generating a plurality of partial products from the
4 multiplicand value and the multiplier value;

5 summing a first subset of the plurality of partial
6 products in a first summation array circuit to thereby produce a
7 first summation value; and

8 summing a remaining subset of the plurality of partial
9 products in a second plurality of adders to thereby produce a
10 second summation value, wherein the remaining subset of the
11 plurality of partial products comprises all of the plurality of
12 partial products not included in the first subset of the plurality
13 of partial products.

1 18. The method as set forth in Claim 17 wherein the first
2 subset comprises even ones of the plurality of partial products.

1 19. The method as set forth in Claim 18 wherein the remaining
2 subset comprises odd ones of the plurality of partial products.

1 20. The method as set forth in Claim 19 wherein each of the
2 first and second pluralities of adders comprises a carry-save
3 adder.